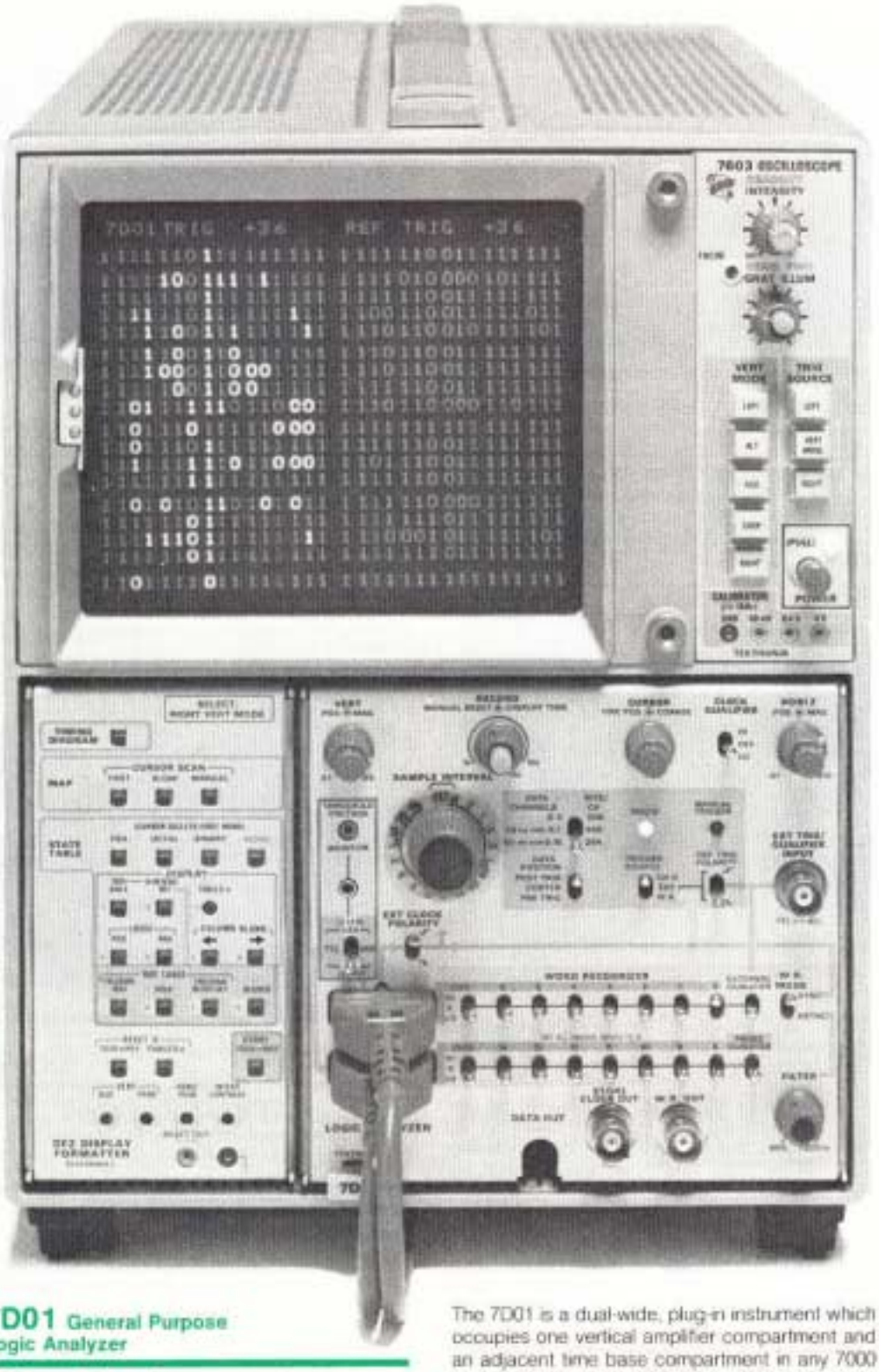

7D01 General Purpose Logic Analyzer

- 16 Stored Channels
- Up to 1024 Words Deep
- State or Timing
- Up to 100 MHz Sample Rate
- High Impedance Probes
- 18 Bit Word Recognizer
- Clock Qualifier

The 7D01 is a dual-wide, plug-in instrument which occupies one vertical amplifier compartment and an adjacent time base compartment in any 7000 Series Oscilloscope Mainframe. With this compatibility, you can configure a total logic analysis system. Using a four-wide mainframe oscilloscope, you can combine your logic analyzer with your analog oscilloscope and display the outputs of both at the same time.

Display Formatters

There are two Display Formatters available wit the 7D01 Logic Analyzer—the DF1 and DF2. Bot offer Timing, Mapping, and State Table Displays in Binary, Hexadecimal and Octal formats. The DF2 offers additional formats for IEEE-488/GPI and ASCII.

The Display formatters are dedicated for use wit the 7D01. They provide complete alphanumeri character generation, so that the logic analysis package can be used in mainframes without CRT readout (mainframe Option 01).

There are also two modes of automatic data acquisition in the DF1 and DF2 which compare the entire 7D01 memory to the reference memory. If a difference is detected, the difference and location will be intensified in the display, read out at the top of the CRT, and the number of resets required to find the error will be displayed. This function, called RESET IF 7D01 — REF, allows fu comparison of stored and newly acquired data. To compare only the tables selected by the cursor control, use RESET IF TABLES —.

Digital Latches

The DL2 and DL502 Digital Latches extend the 7D01 Logic Analyzer's measurement capabilities by detecting narrow pulses in a data stream that cannot be captured by a logic analyzer alone. Operating in an asynchronous mode, the 16 channel Digital Latches can detect spikes or glitches between system clock edges that are narrower than the sample clock interval or as narrow as 5 ns.

7D01 CHARACTERISTICS

The 7D01 acquires 4, 8, or 16 Ch of data and stores the data in a 4 k memory. Data storage format is selectable as 4 Ch X 1016 bits, 8 Ch X 508 bits, or 16 Ch X 254 bits.

Data sampling can be asynchronous (internal clock) or synchronous (external clock). In asynchronous modes, sampling rate can be selected up to 100 MHz in the 4 Ch mode, up to 50 MHz in the 8 Ch mode, or up to 20 MHz in the 16 Ch mode. External sampling clocks up to 50 MHz can be used in the 4 and 8 Ch modes, and up to 25 MHz in the 16 Ch mode.

SIGNAL INPUTS

Clock, Qualifier, and Data Input Source—Two multi-lead P6451 Probes provide connections for 9 Ch (9 input and ground) each. Ch 0-7 and clock are through probe 1, and Ch 8-15 and qualifier are through probe 2. Each probe attaches through a 25 pin connector at the 7D01 front panel.

Clock Qualifier —	Setup	Hold
P6451	20 ns	0 ns
*External	11 ns	7 ns

*Measured at external BNC jack. For 0 ns hold time, 42 inch BNC coaxial cable is recommended.

Input Impedance — 1 MΩ paralleled by 5 pF (at probe head).

Threshold at Probe Tips — Front panel switch selects fixed TTL (+1.4 V, ±0.2 V), variable (±12 V) or split (variable for top probe, TTL for bottom probe). Front panel jack monitors variable threshold only.

Minimum Logic swing — 500 mV plus 2% of threshold voltage p-p or less, centered on the threshold voltage.

Maximum Logic Swing — ±40 V or less, to at least threshold voltage plus 10 V. (Max non-destructive input, ±40 V.)

MEMORY

Storage — 4096 bits.

Format — Front panel selectable.

Data Channels Displayed	Bits per Channel
0-3	1016
0-7	508
0-15	254

SAMPLING RATE

Asynchronous (internal clock) — Sampling intervals are selectable from 10 ns to 5 ms in 18 steps using a 1-2-5 sequence.

Data Channels Displayed	Maximum Sampling Rate	Minimum Sampling Interval*	Min. Data Pluse Width*
0-3	100 MHz	10 ns	15 ns
0-7	50 MHz	20 ns	25 ns
0-15	20 MHz	50 ns	55 ns

*Minimum data pulse width to insure recording is one sample interval ± 5 ns.

Syncheonous (external clock) — + or − edge of clock pulse can be selected to initiate sample.

Data Channels Displayed	Max. Clock Freq.	Minimum Clock Width*	Data Set-up Time Required	Data Hold Time Required
0-3	50 MHz	10 ns	20 ns	0
0-7	50 MHz	10 ns	20 ns	0
0-15	25 MHz	20 ns	23 ns	0

*High and low clock width.

WORD RECOGNIZER

Word Recognizer — 16 data inputs, Probe Qualifier and External Qualifier. Output is true when input conditions match set-logs (HI, X, LO).

Asynchronous Mode

Format	Minimum Input Pulse Width (Asynchronous Mode)
Any Single Channel	10 ns or less
Channels 0-3	15 ns or less
Any Other Combination	20 ns or less

Synchronous Mode

Characteristic	Time Requirement
Minimum Setup Time	12.5 ns or less
Minimum Hold Time	8.5 ns or less

Async Filter — Rejects recognized words that remain true for less than an operator selected time period. Period is variable from 10 ns to 300 ns.

W.R. Out Connector — A recognized word produces a displayed trigger marker and a front panel output for triggering external circuitry.

Characteristic	Requirement
HI Level	≥1.9 V
LO Level	≤0.1 V
Impedance (Rising Edge)	50 Ω ±10%

TRIGGER

Source — Three-position switch provides selection of trigger source from among channel 0, external (External Trigger/Qualifier Input), or internal word recognizer. A display can also be obtained with front panel MANUAL TRIGGER pushbutton.

Channel 0 — Triggers on rising edge of CH 0 data.

External Trigger/Qualifier Input Connector (EXT TRIG/-QUALIFIER INPUT) —

Characteristics	Requirement
Threshold	+1.4 V, ±0.2 V (TTL Level)
Minimum Pulse Width	15 ns
Maximum Safe Input Voltage	−5 V or less, to at least +10 V

Triggered Light — Indicates display trigger has occurred.

CURSOR

Word Selection — Cursor appears as a movable second intensified spot on the CRT display. It is used to select and mark a word.

Coarse and Fine Position Controls — Coarse control moves cursor in increments of 16 sample intervals. Fine control moves cursor in increments of 1 sample interval.

Cursor to Trigger Position CRT Readout — The difference in sample interval bits between cursor position and trigger position is displayed by the CRT readout at the top, right-hand portion of the CRT graticule (e.g., TRIG + XXX).

Cursor Position Binary Data — The logic state of each displayed channel coincident with the cursor position is displayed in Binary by the readout at the bottom of the CRT (HI = 1, LO = 0).

Trigger Intensified Marker — Intensified zone indicating the trigger point, selectable by a switch (DATA POSITION).

Data Position Switch Setting	Intensified Zone Location
Pre-trigger	Near extreme right of display
Center-trigger	Near center of display
Post-trigger	Near extreme left of display

Trigger Intensified Marker Accuracy — Position of intensified zone with respect to word recognizer output.

Sample Interval Control Setting	Maximum Bit Error
10 ns	±4 bits
20 ns	±3 bits
50 ns to 5 ms	±1 bit

POWER

Line Voltage Ranges — Determined by the 7000 Series Oscilloscope Mainframe.

Power Consumption — 32 W at nominal line voltage.

ENVIRONMENTAL

Temperature — Operating: 0°C to +40°C. Nonoperating: −40°C to +75°C.

Altitude — Operating: to 15,000 feet. Nonoperating: to 50,000 feet.

Vibration — With the 7D01 and DF1 or DF2 combined, frequency swept from 10 to 55 cps at one minute per sweep. Vibrate for 15 minutes along each of the 3 major axes at 0.015 inch total displacement. Hold 3 minutes at any major resonance, or if none, at 55 cps. Total time, 54 minutes.

Shock — Operating and nonoperating: 30 g's, 1/2 sine 11 ms duration, 2 shocks in each direction along 3 major axes, for a total of 12 shocks.

INCLUDED ACCESSORIES

Two P6451 Data Input Probes (010-6451-03).

DF1 CHARACTERISTICS

The DF1 reformats the output of the 7D01 in a choice of five display formats including Timing, Mapping and state table displays in Binary, Hexadecimal and Octal. It imposes no significant electrical characteristics on the 7D01 which affect measurement parameters.

DF2 CHARACTERISTICS

The DF2 reformats the output of the 7D01 in a choice of seven display formats including Timing, Mapping and state table displays in Binary, Hexadecimal, Octal, ASCII and IEEE-488 GPIB. It imposes no significant electrical characteristics on the 7D01 which affect measurement parameters.

INCLUDED ACCESSORIES

GPIB Probe Adapter for the P6451 (103-0209-00). (A 24 pin IEEE Standard Connector with quick connection to the P6451 Probe Head.)

DL2 CHARACTERISTICS

The 16 channel DL2 adds the 7D01 measurement capabilities by detecting narrow asynchronous pulses of less than one sample interval or as narrow as 5 ns in a data stream. The DL2 plugs into any compartment of a 7000 Series Mainframe. Two 25 pin connectors connect the DL2 with the 7D01. Data is acquired via two P6451 Probes which plug into the front panel of the DL2.

Minimum Pulse Width to Initiate Latch — 5 ns.

Minimum Amplitude to Initiate Latch — 500 mV centered at threshold.

Minimum Sample Interval Asynchronous Clock — 50 ns.

ORDERING INFORMATION

7D01F Logic Analyzer (7D01 and DF1 Display Formatter)

7D01F2 Logic Analyzer (7D01 and DF2 Display Formatter)

7D01 Logic Analyzer

DF1 Display Formatter

DF2 Display Formatter

DL2 Digital Latch

DL 502 Digital Latch

7603 Oscilloscope*

Option 01 (Deletes one readout board)

7704A Oscilloscope*

Option 01 (Deletes one readout board)

To modify your present 7D01 to include the new clock qualifier feature order clock Qualifier* modification kit.

040-0891-00

*See pages 155 through 175 in this catalog for details on these and additional 7000 Series Mainframes. See pages 183 through 204 for details on complementary 7000 Series Plug-ins.